Abstract of the Disclosure

A delay locked loop (DLL) in a semiconductor device, includes an clock buffer receiving an external clock signal and an inverted clock signal and outputting first and second internal clock signals to be used in the DLL circuit; and a variable clock divider receiving the second internal signal from the clock buffer and variably dividing the second internal clock signal to have a predetermined pulse width according to a control signal based on a column address strobe (CAS) latency, which is set according to a frequency of the external clock signal, wherein the control signal is initially set to have a first logic level and is enabled to a second logic level when the CAS latency corresponds to a high frequency.